IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Hongyong Zhang	Art Unit	: 2814
Serial No.	: 09/362,808	Examiner	: Shrinivas H. Rao
Filed	: July 28, 1999	Conf. No.	: 7320
Title	: METHOD OF FABRICATING SEMICONDUCTOR DEVICE		

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BRIEF ON APPEAL

(1) Real Party in Interest

Semiconductor Energy Laboratory Co., Ltd., the assignee of this application, is the real party in interest.

(2) Related Appeals and Interferences

There are no related appeals or interferences.

(3) Status of Claims

Claims 1-49 are currently pending, with claims 1, 6, 10, 14, 19, 24, 44 and 47 being independent. Claims 1-13, 33 and 34 are allowed. Claims 14-30, 35-37 and 41-49 have been rejected, and this rejection is being appealed.

(4) Status of Amendments

The claims were not amended after the final rejection of May 4, 2006.

(5) Summary of Claimed Subject Matter

In the discussion below, reference numerals and references to particular portions of the specification are inserted for illustrative purposes only and are not meant to be limit the scope of the claims.

Independent claim 14 is directed to a semiconductor device that includes a semiconductor layer (102) formed over a substrate (101) having an insulating surface and including at least channel, source and drain regions (113, 109 and 110). (See the application at Figs. 1(A) to 1(D)

and page 7, lines 1-9 and page 8, lines 11-16.) The device also includes an insulating film (103) on the semiconductor layer, a gate electrode (108) over the insulating film, at least a first interlayer insulating film (114) over the insulating film and over the gate electrode, and a second interlayer insulating film (115) over the first interlayer insulating film. (See the application at Figs. 1(A) to 1(D) and page 7, lines 10-14 and page 9, lines 11-16 and 26-29.) There is at least one contact hole having a tapered section in the first and second interlayer insulating films and the insulating film. (See the application at Fig. 2(A) and page 10, line 26 to page 11, line 10.) An electrode (205) is formed on the contact hole and connected with one of the source and drain regions through the contact hole. (See the application at Fig. 2(D) and page 12, lines 11-13.) A taper angle β of an inner surface of the second interlayer insulating film in the contact hole with respect to a major surface of the semiconductor layer is larger than a taper angle α of an inner surface of the first interlayer insulating film in the contact hole with respect to the major surface of the semiconductor layer. (See the application at Fig. 3 and page 4, lines 14-19.)

Independent claim 19 recites a semiconductor device similar to that of claim 14. The semiconductor device differs from that of claim 14 in that claim 19 does not recite a substrate and recites that the semiconductor region includes a channel region (113), at least one low doped impurity region (111 or 112), and at least one high doped impurity region (109 or 110), with the high doped impurity region being adjacent to the channel region with the low doped impurity region interposed therebetween. (See the application at Fig. 1(C) and page 9, lines 11-16.) Claim 19 further recites that the contact hole exposes a portion of the high doped region and includes a first hole in the second interlayer insulating film, a second hole in the first interlayer insulating film, and a third hole in the insulating film, with the contact hole having a tapered section such that the first hole has a larger cross section than the second hole, and the second hole has a larger cross section than the third hole. (See the application at Figs. 2(C) and 4.) Claim 19 also recites that edges of the second interlayer insulating film in the contact hole are rounded off, and that angles of the tapered section of the contact hole decrease successively from the second interlayer insulating film toward the first interlayer insulating film. (See the application at Fig. 4 and page 14, lines 9-12.) Finally, claim 19 recites that a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films. (See the application at page 10, lines 22-23.)

Independent claim 24 recites a semiconductor device that includes a substrate like the device of claim 14 and low and high doped impurity regions like the device of claim 19. Like claim 19, claim 24 also recites that the device includes a gate electrode over the insulating film, at least a first interlayer insulating film over the insulating film and over the gate electrode, a second interlayer insulating film over the first interlayer insulating film, a contact hole in the interlayer insulating films and the insulating film for exposing a portion of the high doped impurity region and having a tapered section, and an electrode formed on the contact hole and connected with one of the source and drain regions through the contact hole. Like claim 19, claim 24 also recites that edges of the interlayer insulating film in the contact hole are rounded off.

Independent claim 44 recites a semiconductor device that includes a metal layer (104 or 108) formed over a glass substrate (101), a first insulating film (114) over the metal layer, and a second insulating film over the first insulating film (115). (See the application at Figs. 1(A) to 1(D); page 7, lines 1-6, 13-14 and 27-28; page 8, lines 17-18; and page 9, lines 26-29.) The device also includes a first opening in the first insulating film to expose a portion of the metal layer, and a second opening in the second insulating film to expose a portion of the metal layer and a portion of the first insulating film. (See the application at Fig. 2C.) A first taper angle of the first insulating film in the first opening is smaller than a second taper angle of the second insulating film in the second opening. (See the application at Fig. 3 and page 4, lines 14-19.)

Independent claim 47 recites a semiconductor device that includes the properties of the device of claim 44. Claim 47 further recites that a thickness of the first insulating film is less than one third of a total thickness of the first and second insulating films. (See the application at page 10, lines 22-23.)

(6) Grounds of Rejection to be Reviewed on Appeal

Claims 14-30, 35-37 and 41-49 have been rejected as being unpatentable over Fu (U.S. Patent No. 4,342,617) in view of Sasaki (U.S. Patent No. 4,404,733) and Lin (U.S. Patent No. 5,841,195).

(7) Argument

a. The rejection of claims 14, 19, 44 and 47, and their dependent claims, should be reversed because neither Fu, Sasaki, Lin, nor any proper combination of the three describes or suggests a first interlayer insulating film having a smaller taper angle and over an insulating film and a gate electrode, and a second interlayer insulating film having a larger taper angle and over the first interlayer insulating film, as recited in claims 14, 19, 44 and 47.

As noted above, claim 14 is directed to a semiconductor device that includes a semiconductor layer formed over a substrate having an insulating surface and including at least channel, source and drain regions, an insulating film on the semiconductor layer, a gate electrode over the insulating film, a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating film over the first interlayer insulating film. The device also includes at least one contact hole having a tapered section and formed in the first and second interlayer insulating films and the insulating film, and an electrode formed on the contact hole and connected with one of the source and drain regions through the contact hole. Claim 14 further recites that a taper angle β of an inner surface of the second interlayer insulating film in the contact hole with respect to a major surface of the semiconductor layer is larger than a taper angle α of an inner surface of the first interlayer insulating film in the contact hole with respect to the major surface of the semiconductor layer. Thus, claim 14 requires the second interlayer insulating film to be over the first interlayer insulating film, and further requires the first interlayer insulating film to be over the insulating film and the gate electrode (which, in turn, are over the semiconductor layer formed over the substrate). Thus, according to claim 14, the first interlayer insulating film (which has the smaller taper angle) is between the substrate and the second interlayer insulating film (which has the larger taper angle).

With respect to claim 14 and its dependent claims, appellant requests reversal of this rejection because neither Fu, Sasaki, Lin, nor any proper combination of the three describes or suggests a first interlayer insulating film having a smaller taper angle and over an insulating film and a gate electrode, and a second interlayer insulating film having a larger taper angle and over the first interlayer insulating film, as recited in claim 14.

The rejection relies on Lin as showing this feature. In particular, the rejection provides two different explanations as to how Lin is believed to describe the recited arrangement of taper

angles. First, in the body of the rejection, the rejection appears to indicate that the layers 16/18 together have the recited larger taper angle β, and that the layers 20/22 together have the recited smaller taper angle α. Second, in the response to arguments section, the action appears to argue that one of the layers 16/18 has the recited larger taper angle β and the other has the recited taper angle α, or that one of the layers 20/22 has the recited larger taper angle β and the other has the recited taper angle α. Each of these explanations is incorrect.

As shown above, claim 14 requires the second interlayer insulating film to be over the first interlayer insulating film, and further requires the first interlayer insulating film to be over the insulating film and the gate electrode (which, in turn, are over the semiconductor layer formed over the substrate). Thus, according to claim 14, the first interlayer insulating film (which has the smaller taper angle) is between the substrate and the second interlayer insulating film (which has the larger taper angle).

With reference to Fig. 6 of Lin, if the layer 16 of Lin is said to correspond to the recited first interlayer insulating film, the layer 18 could not qualify as the second interlayer insulating film because the layers 16 and 18 have the same taper angle. Nor could either of the layers 20 and 22 qualify, since both of these layers have a smaller taper angle than layer 16, which is located between these layers and the substrate, while the claim requires a larger taper angle.

If the layer 18 of Lin is said to correspond to the recited first interlayer insulating film, the layer 16 could not qualify as the second interlayer insulating film because the layer 18 is not between the layer 16 and the substrate, and because the layers 16 and 18 have the same taper angle. Nor could either of the layers 20 and 22 qualify, since both of these layers have a smaller taper angle than the layer 18, which is located between these layers and the substrate, while the claim requires a larger taper angle.

If the layer 20 of Lin is said to correspond to the recited first interlayer insulating film, neither of the layers 16 and 18 could qualify as the second interlayer insulating film because claim 20 is not between either of the layers 16 and 18 and the substrate. The layer 22 also could not qualify as the second interlayer insulating film because the layers 20 and 22 have the same taper angle.

If the layer 22 of Lin is said to correspond to the recited first interlayer insulating film, none of the layers 16, 18 and 20 could qualify as the second interlayer insulating film because the layer 22 is not between any of the layers 16, 18 and 20 and the substrate.

Accordingly, since no possible combination of the layers 16-22 of Lin satisfy the relationship set forth in claim 14, Lin does not satisfy this relationship and the rejection of claim 14 and its dependent claims should be reversed.

Like claim 14, each of independent claims 19, 44 and 47 recites an arrangement in which a first insulating film (which has the smaller taper angle) is between a substrate and a second insulating film (which has the larger taper angle). Accordingly the rejection of claims 19, 44 and 47, along with their dependent claims, should be reversed for the reasons discussed above with respect to claim 14.

<u>b. The rejection of claim 24 and its dependent claims should be reversed because neither Fu, Sasaki, Lin, nor any proper combination of the three describes or suggests a semiconductor layer formed over a substrate having an insulating surface and having a channel region, at least one low doped impurity region, and at least one high doped impurity region that is adjacent to the channel region with the low doped impurity region interposed therebetween, as recited in claim 24.</u>

Claim 24 recites a semiconductor device that includes, among other features, a semiconductor layer formed over a substrate having an insulating surface and having a channel region, at least one low doped impurity region, and at least one high doped impurity region that is adjacent to the channel region with the low doped impurity region interposed therebetween. As best understood, the rejection asserts that Fig. 2e of Sasaki shows this feature with the regions 15, 16 being the low doped impurity regions and the regions 15', 16' being the high doped impurity regions, and the region between the regions 15, 16 being the channel region. However, in Sasaki, the regions 15, 16, 15' and 16' are formed in the substrate 11. As such, Sasaki does not describe or suggest the semiconductor layer recited in claim 24. Nor does there appear to be any motivation to combine Fu, Sasaki and Lin to somehow arrive at this feature. Accordingly, the rejection of claim 24 and its dependent claims should be reversed.

For the reasons presented above, the rejections should be reversed.

The fee in the amount of $620 in payment of the brief fee ($500) and the one-month extension fee ($120) is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Appendix of Claims

1. (Previously Presented) A semiconductor device comprising:

a semiconductor having at least channel, source and drain regions;

an insulating film formed on said semiconductor;

a gate electrode over the insulating film;

a first interlayer insulating film over said insulating film and the gate electrode;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film that surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor, said portion of said insulating film and a portion of said first interlayer insulating film that surrounds said second opening,

wherein edges of at least said third opening are rounded off, and

wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

2. (Previously Presented) A device according to claim 1 wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor in the second opening.

3. (Previously Presented) A device according to claim 1, wherein said insulating film comprises silicon oxide.

4. (Previously Presented) A device according to claim 1, wherein said first and second interlayer insulating films comprise a material selected from the group consisting of silicon nitride and organic resin.

5. (Previously Presented) A device according to claim 1, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

6. (Previously Presented) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface, said semiconductor layer having at least channel, source and drain regions;

a gate insulating film over said semiconductor layer;

a gate electrode over the gate insulating film;

a first interlayer insulating film over said gate insulating layer and the gate electrode

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said gate insulating film;

a first opening in said gate insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said gate insulating film that surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said gate insulating film and a portion of said first interlayer insulating film that surrounds said second opening,

wherein edges of at least said third opening are rounded off, and

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor layer in the second opening.

7. (Previously Presented) A device according to claim 6, wherein said gate insulating film comprises silicon oxide.

8. (Previously Presented) A device according to claim 6, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

9. (Previously Presented) A device according to claim 6, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

10. (Previously Presented) A semiconductor device comprising:

a semiconductor having at least channel, source and drain regions;

an insulating film on said semiconductor;

a gate electrode over the insulating film;

a first interlayer insulating film over said insulating film and the gate electrode;

a second interlayer insulating film on said first interlayer insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor and a portion of said insulating film that surrounds said first opening;

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor, said portion of said insulating film and a portion of said first interlayer insulating film that surrounds said second opening; and

an electrode formed on said first, second, and third openings and connected with one of said source and drain regions through said first, second, and third openings,

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to a major surface of said semiconductor in the second opening, and

wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

11. (Previously Presented) A device according to claim 10, wherein said insulating film comprises silicon oxide.

12. (Previously Presented) A device according to claim 10, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

13. (Previously Presented) A device according to claim 10, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

14. (Previously Presented) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface and including at least channel, source and drain regions;

an insulating film on said semiconductor layer;

a gate electrode over the insulating film;

at least a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating film over the first interlayer insulating film;

at least one contact hole in said first and second interlayer insulating films and said insulating film, said contact hole having a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein a taper angle β of an inner surface of the second interlayer insulating film in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of the first interlayer insulating film in the contact hole with respect to said major surface of said semiconductor layer.

15. (Previously Presented) A device according to claim 14, wherein said insulating film comprises silicon oxide.

16. (Previously Presented) A device according to claim 14, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

17. (Previously Presented) A device according to claim 14, wherein said second interlayer insulating films has a dry etching rate higher than said first interlayer insulating layer.

18. (Previously Presented) A device according to claim 14, wherein angles of the tapered section of the contact hole decrease successively from the second interlayer insulating layer toward a first interlayer insulating layer.

19. (Previously Presented) A semiconductor device comprising:

a semiconductor having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor;

a gate electrode over the insulating film;

at least a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating film over the first interlayer insulating film; and

a contact hole in said first and second interlayer insulating films and said insulating film for exposing a portion of said high doped impurity region, said contact hole including a first hole in the second interlayer insulating film, a second hole in the first interlayer insulating film, and a third hole in the insulating film, the contact hole having a tapered section such that the first hole has a larger cross section than the second hole, and the second hole has a larger cross section than the third hole,

wherein edges of said second interlayer insulating film in said contact hole are rounded off,

wherein angles of the tapered section of the contact hole decrease successively from the second interlayer insulating film toward the first interlayer insulating film, and

wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

20. (Previously Presented) A device according to claim 19 wherein said insulating film comprises silicon oxide.

21. (Previously Presented) A device according to claim 19 wherein at least one of said first and second interlayer insulating films comprises a material selected from the group consisting of silicon nitride and organic resin.

22. (Previously Presented) A device according to claim 19 wherein said low doped impurity region includes phosphorus at a dose of 0.1 to 5×10^{14} atoms/cm^2.

23. (Previously Presented) A device according to claim 19 wherein said high doped impurity region includes phosphorus at a dose of 0.2 to 5×10^{15} atoms/cm^2.

24. (Previously Presented) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface and having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

a gate electrode over the insulating film;

at least a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating film over the first interlayer insulating film;

a contact hole in said interlayer insulating films and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein edges of said interlayer insulating film in said contact hole are rounded off.

25. (Previously Presented) A device according to claim 24, wherein a taper angle β of an inner surface of the second interlayer insulating film in the contact hole with respect to a major

surface of said semiconductor layer is larger than a taper angle α of an inner surface of first interlayer insulating film in the contact hole with respect to said major surface of said semiconductor layer.

26. (Previously Presented) A device according to claim 24, wherein angles of the taper shape of the contact hole decrease successively from the second interlayer insulating film toward the first interlayer insulating film.

27. (Previously Presented) A device according to claim 24 wherein said insulating film comprises silicon oxide.

28. (Previously Presented) A device according to claim 19 wherein at least one of said first and second interlayer insulating films comprises a material selected from the group consisting of silicon nitride and organic resin.

29. (Previously Presented) A device according to claim 24 wherein said low doped impurity region includes phosphorus at a dose of 0.1 to 5 x 10^{14} atoms/cm^2.

30. (Previously Presented) A device according to claim 24 wherein said high doped impurity region includes phosphorus at a dose of 0.2 to 5 x 10^{15} atoms/cm^2.

31. (Previously Presented) A device according to claim 1, wherein edges of said first opening are rounded off.

32. (Previously Presented) A device according to claim 1, further comprising an electrode connected with one of said source and drain regions through said first, second, and third openings.

33. (Previously Presented) A device according to claim 6, wherein edges of said first opening are rounded off.

34. (Previously Presented) A device according to claim 6, further comprising an electrode connected with one of said source and drain regions through said first, second, and third openings.

35. (Previously Presented) A device according to claim 19, wherein edges of said insulating film in said contact hole are rounded off.

36. (Previously Presented) A device according to claim 19, further comprising an electrode connected with one of said source and drain regions through said contact hole.

37. (Previously Presented) A device according to claim 24, wherein edges of said insulating film in said contact hole are rounded off.

38. (Previously Presented) A device according to claim 6, wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

39. (Previously Presented) A device according to claim 14, wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

40. (Previously Presented) A device according to claim 24, wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

41. (Previously Presented) A device according to claim 14, wherein said first interlayer insulating film is formed on and in contact with the insulating film, and over the gate electrode, and said second interlayer insulating film is formed on and in contact with said first interlayer insulating film.

42. (Previously Presented) A device according to claim 19, wherein said first interlayer insulating film is formed on and in contact with the insulating film, and over the gate electrode, and said second interlayer insulating film is formed on and in contact with said first interlayer insulating film.

43. (Previously Presented) A device according to claim 24, wherein said first interlayer insulating film is formed on and in contact with the insulating film, and over the gate electrode, and said second interlayer insulating film is formed on and in contact with said first interlayer insulating film.

44. (Previously Presented) A semiconductor device comprising:

a metal layer formed over a glass substrate;

a first insulating film over the metal layer;

a second insulating film over the first insulating film;

a first opening in the first insulating film to expose a portion of the metal layer; and

a second opening in the second insulating film to expose a portion of the metal layer and a portion of the first insulating film,

wherein a first taper angle of the first insulating film in the first opening is smaller than a second taper angle of the second insulating film in the second opening.

45. (Previously Presented) The semiconductor device according to claim 44, wherein said first insulating film and said second insulating film are formed from a same material.

46. (Previously Presented) The semiconductor device according to claim 44, wherein at least any one of said first insulating film and said second insulating film are formed from silicon nitride.

47. (Previously Presented) A semiconductor device comprising:

a metal layer formed over a glass substrate;

a first insulating film over the metal layer;

a second insulating film over the first insulating film;

a first opening in the first insulating film to expose a portion of the metal layer; and

a second opening in the second insulating film to expose a portion of the metal layer and a portion of the first insulating film,

wherein a thickness of the first insulating film is less than one third of a total thickness of the first and second insulating films, and

wherein a first taper angle of the first insulating film in the first opening is smaller than a second taper angle of the second insulating film in the second opening.

48. (Previously Presented) The semiconductor device according to claim 47, wherein said first insulating film and said second insulating film are formed from a same material.

49. (Previously Presented) The semiconductor device according to claim 47, wherein at least any one of said first insulating film and said second insulating film are formed from silicon nitride.

Evidence Appendix

None.

Related Proceedings Appendix

None.